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ASX RELEASE

4 November 2021

4DS TECHNICAL UPDATE

- **Extensive additional testing of Third Non-Platform Lot wafers with up to one order of magnitude boost in read speed has identified a potentially modest degradation in endurance**
- **A Third Platform Lot memory stack etch mask modification is needed and further optimization of the etch process utilizing this new mask will be required before the Third Platform Lot can be started**
- **After successful completion of the memory stack etch optimization, a Third Platform Lot utilizing imec's megabit memory platform will be started.**
- **4DS and imec have negotiated a one year extension to their Collaboration agreement**

4DS Memory Limited (ASX:4DS) (**4DS**) (the **Company**), today advises the results of additional testing of the Third Non-Platform Lot and Second Platform Lot wafers.

Background to Non-Platform Lots to date

Since 2020, the focus of the Non-Platform Lots has been to fine tune and optimize the process parameters of 4DS' memory cell technology for Storage Class Memory and on 17 August 2021 the Company released a summary of the results for all three Non-Platform Lots.

As announced on 17 August 2021, 4DS demonstrated that fully crystalline PCMO material reduced the cell on-resistance by an order of magnitude compared to the PCMO material fabricated in the Second Non-Platform Lot. This reduction in cell on-resistance directly translated into a significant improvement in read speed.

The Company also stated that this significant performance improvement also meant that full characterization (speed, endurance, retention) of memory cells with this fully crystalline PCMO material requires memory cells operating in a memory array where currents are controlled and limited by access devices.

Storage Class Memory

As there is no established market for Storage Class Memory, the Company continues to explore speed, endurance and retention performance and are quantifying the trade-offs between these parameters. Fully quantifying the trade-offs between these parameters will enable our future users to select the operating space which is most attractive for their future applications that require memory solutions "between" DRAM and NAND.

Updated Analysis following additional testing

Since 17 August 2021, 4DS has continued to improve its test capability to extract additional information from the Third Non-Platform Lot on endurance of its memory cells. Improvement in the Company's test capability has shown that while endurance of these improved cells remains several orders of magnitude better than NAND endurance, it has potentially degraded when compared to the Second Non-Platform Lot performance reported in a Company announcement on 1 February 2021. Part of this degradation may be caused by test related issues resulting from testing the memory cell without an access device.

These testing challenges highlight the need to switch from using Non-Platform Lots to using Platform Lots which include imec access transistors. The Third Platform Lot will also include a test chip: an imec 1 megabit array using 4DS' ReRAM cells.

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4DS expects that the results from the Third Platform Lots will resolve the ambiguity of the endurance test results to date.

imec production of a Third Platform Lot with imec access transistors

imec Non-Platform Lots only support standalone 4DS ReRAM memory cells whilst the Third Platform Lot will include 4DS ReRAM memory cells with imec access transistors. This will enable more precise measurements of endurance and retention at the higher currents that resulted from the process improvements made in the Third Non-Platform Lot.

Following further testing of the Second Platform Lot the Company and imec have engaged in extensive discussions on technical matters regarding these results and the successful manufacture of the Third Platform Lot, which was announced in the 17 August 2021 press release. The additional testing results and the above referenced technical matters are the reason the Company sought a trading halt on 8 October 2021. Subsequently the Company entered into a voluntary trading suspension. The Company has been working very closely with imec to ensure that the Third Platform Lot will deliver the desired technical outcomes.

4DS and imec have now concluded these discussions. The start of the Third Platform Lot is now expected to occur in early 2022 and will be preceded by a memory stack etch mask change and further etch process optimization to resolve the technical issues that resulted in the partial failure of the Second Platform Lot as announced on 17 August 2021. Performing this memory stack etch optimization will result in a three month delay of our time line. Following the successful completion of this work, the Third Platform Lot utilizing imec's megabit memory platform will be started. The expected out-of-fab date is July 2022. Because the processing of the Third Platform Lot will occur in the first half of 2022, the Company has negotiated a one year extension of the current agreement with imec, which was scheduled to expire by 31 December 2021.

imec contract renewal for 2022

imec and 4DS have negotiated to again extend the collaboration agreement to the end of 2022. Under this agreement 4DS has committed to pay imec an additional 600,000 Euro for the first 7 months in 2022. In August 2022 imec and 4DS will review the requirements for the balance of the year.

Whilst the collaboration with imec remains in place imec is entitled to a **capped** royalty of 8% on 4DS' License Income. To date the Company has not made any royalty payments to imec, since payments are **only** due on any licence revenue generated by 4DS or a sale of the Company.

The Company considers this capped royalty as non-material. Under the new amendment to the agreement the royalty is now **capped** at approximately 5 million euro (~AUS$ 7.8 million).

The Board considers this to be a good outcome for shareholders, since royalties are only due after a successful commercialisation of the technology.

It also reinforces that imec has confidence in the success of 4DS' technology.

Stanford Nanofabrication Facility

In parallel, we continue to explore further improvements to our process technology and cell structure in collaboration with Stanford's Nanofabrication Facility which was instrumental in reducing the cycle time of process improvement iterations.

ENDS

Authorised for release by the Board.

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About 4DS

4DS Memory Limited (ASX: 4DS), with facilities located in Silicon Valley, is a semiconductor development company of non-volatile memory technology, pioneering Interface Switching ReRAM for next generation gigabyte storage in mobile and cloud. Established in 2007, 4DS owns a patented IP portfolio, comprising 32 USA patents granted (of which 4 have expired) and 1 patent application, which have been developed in-house to create high-density Storage Class Memory. 4DS has a joint development agreement with Western Digital subsidiary HGST, a global storage leader, which accelerates the evolution of 4DS' technology. 4DS also collaborates with imec, a world-leading research and innovation hub in nanoelectronics and digital technologies. The combination of imec's widely acclaimed leadership in microchip technology and profound software and information and communication technology expertise makes them unique.

For more information, please visit www.4dsmemory.com.