

Annual General Meeting

November 30, 2017





Weebit Nano AT A GLANCE



Listed on the ASX in August 2016



Targeting the storage market which is estimated at > USD\$40B



R&D and HQ in Israel, R&D partnership with CEA-Leti, France



Business & Tech partners – CEA-Leti France & Rice University, USA



Developing next-gen solution based on Silicon Oxide (SiOx) ReRAM

Patents Registered in the USA

KEY INVESTMENT HIGHLIGHTS



MASSIVE STORAGE DEMAND

Exponential increase in demand for memory storage



EXCELLENT DEVELOPMENT RESULTS

Scaled devices with a memory array significantly faster than Flash memory imminent



KEY DEVELOPMENT PARTNERSHIP

CEA-Leti, world-class research institution



MARKET DRIVERS

Content explosion and Artificial Intelligence (AI) are creating new opportunities for memory technologies (e.g. ReRAM)



ON TRACK

Working 40nm cells achieved before year end of 2017, on track for 1Mbit by mid 2018



ADDRESSABLE MARKET

> USD\$40B+

SHARE INFORMATION

CAPITAL STRUCTURE

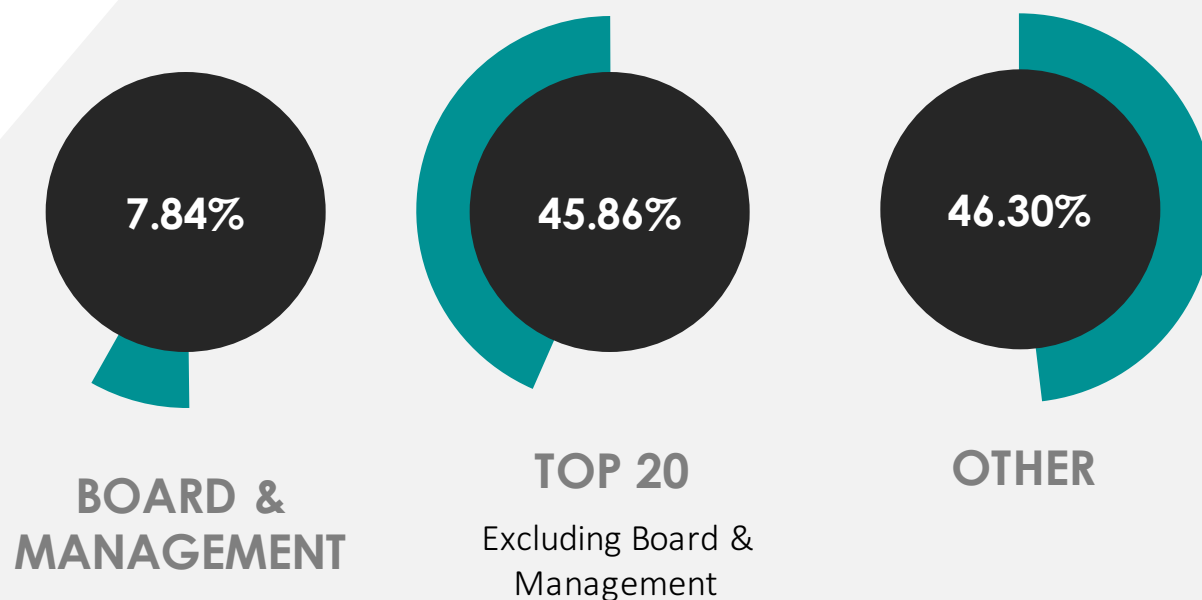
01	ASX Code: WBT
02	Share price: 7.6c ¹
03	Shares on issue: 1391m
04	Options: 201m ²
05	Market cap*: A\$106m
06	Cash (30 Sep 17): \$1.18m ³

1. As of 27 Nov 2017

2. Including Options subject to approval at AGM and existing Options & Performance Shares

3. Does not include net proceeds of \$2.5m Capital Raise completed on 3 October 2017 nor does it include the proceeds from the 48.7m Options exercised in November 2017

SHAREHOLDING BREAKDOWN



LEADERSHIP TEAM

INVENTOR



Prof. James Tour

Scientist of the Year 2013
R&D magazine

Inducted to the National
Academy of inventors

Feynman prize in
Nano science

CHAIRMAN



David Perlmutter

Ex-Intel EVP
IEEE Fellow

Has led intel into
the Data Center

Brought to Market:
Centrino™ mobile
technology

CEO



Coby Hanoch

Extensive management
and sales experience

37 years in the
semiconductor domain

Enabled Verisity and Jasper
acquisitions

VP R&D



Amir Regev

Two decades in
Semiconductors engineering

45nm NOR Flash Technology
Development at Micron

Was part of Automotive
division at Intel

THE NEW CEO

- 37 years in the semiconductor space
 - 15 years in engineering/engineering management
 - 22 years in CEO and VP Sales roles
- Verisity SVP WW Sales
 - \$315M acquisition by Cadence
- Jasper VP WW Sales
 - \$170M acquisition by Cadence
- Packetlight CEO
- EDAcon Partners





WEEBIT ReRAM TECHNOLOGY

Designed for next generation technology



ENERGY EFFICIENCY

Ultra Low Power



SPEED – READ AND WRITE

Significantly faster than Flash



INTEGRATION

Bringing the memory closer to the processor

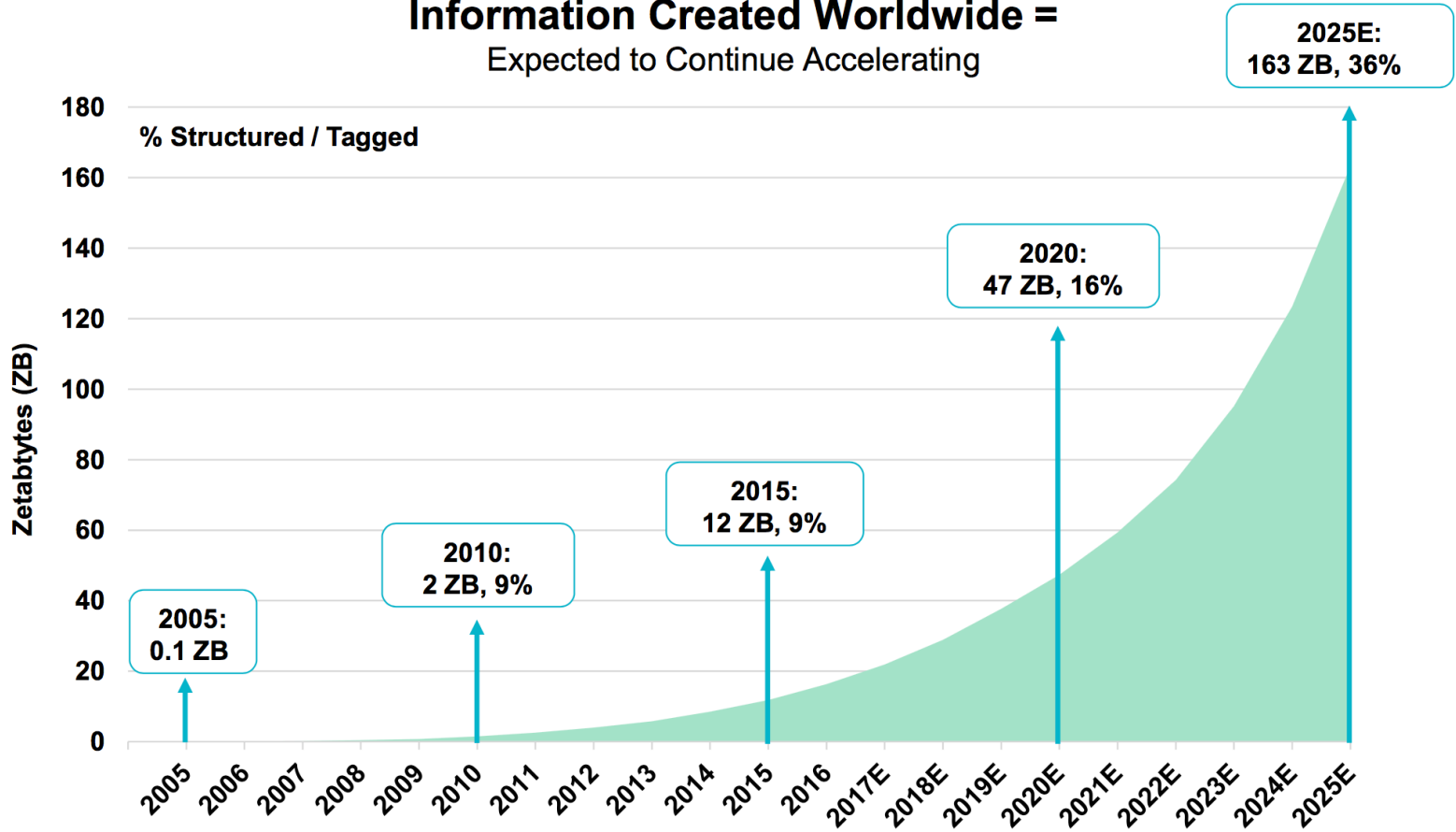


LOW COST / NO SPECIAL MANUFACTURING TECHNOLOGY & NO RETOOLING

Manufacturability - minimum added process steps and cost

DATA EXPLOSION IS COMING

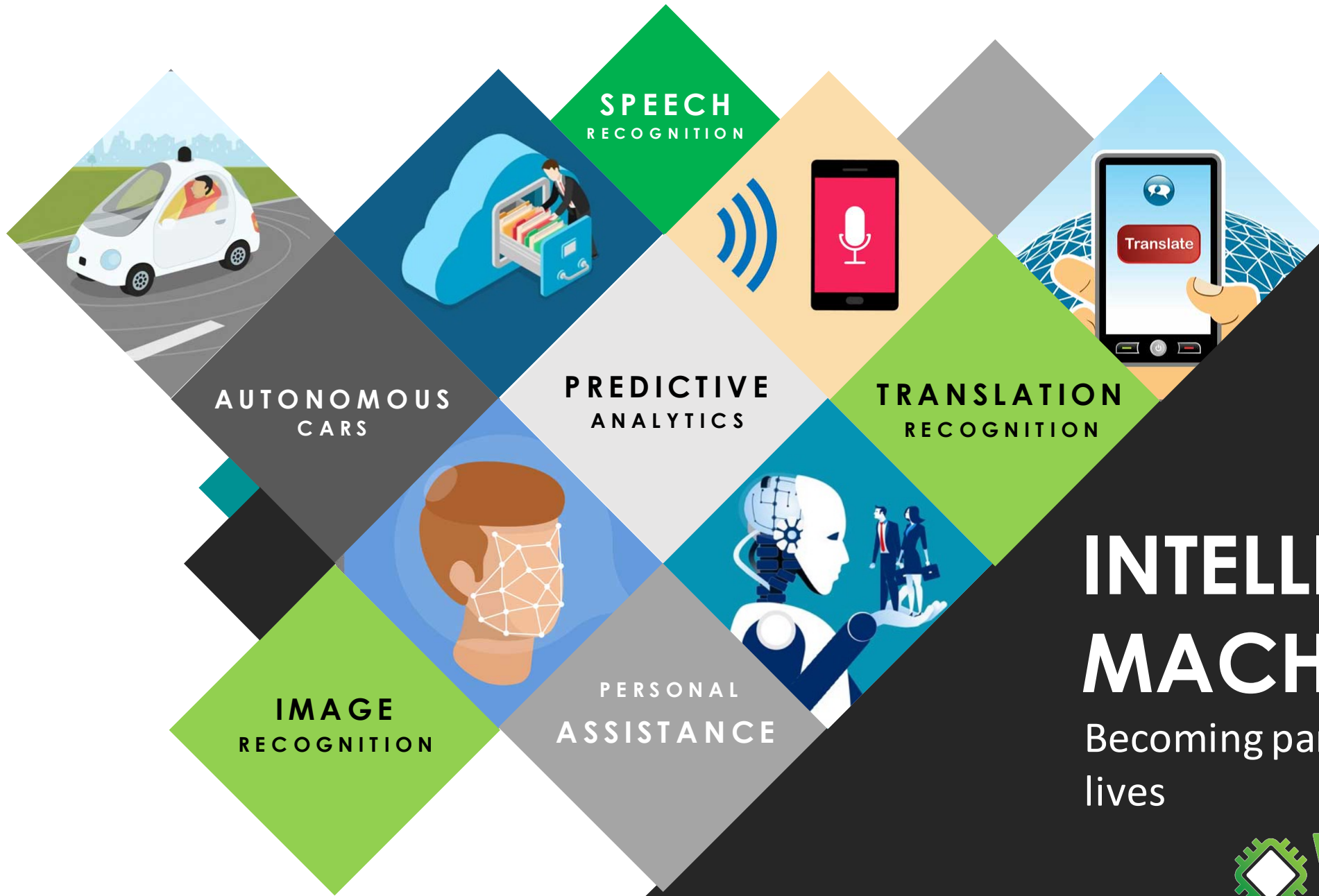
Information Created Worldwide =
Expected to Continue Accelerating



“We live in a *new data economy* that will generate huge amounts of data. Autonomous vehicles and the network that connects them will generate lots of data. The *Internet of Things* will also be a big source of data. *Cognitive computing* and *artificial intelligence* will be used to analyze much of this data”

Marc Durcan
Micron CEO Micron Feb 2017





INTELLIGENT MACHINES

Becoming part of our everyday lives

WEEBIT SOLUTIONS FOR THE INDUSTRY

Building smaller cell is better/cheaper

MORE INFORMATION STORED IN A PIECE OF SILICON WITH A FASTER WRITE AND READ

SILICON OXIDE

Weebit NANO NEXT-GEN MEMORY SOLUTION

- ✓ Fab Friendly – 50 year process & manufacturing experience
- ✓ Compatibility – well integrated with existing proven processes

MANUFACTURABLE ANYWHERE

- ✓ Any Fab – no need for specialised foundry
- ✓ Any Tool – no need for special tool
- ✓ Any process – no need for special process

H																			He
Li	Be																		Ne
Na	Mg																		Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr		
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe		
Cs	Ba	Lu	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn		
Fr	Ra	Lr	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg	Cn								
			Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu			
			Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr			

■ Not Used in Semiconductor Fabs

■ Used in Semiconductor Fabs

Shortest time to market, cheaper, Faster

RERAM COMPETITIVE LANDSCAPE



**Market
Capitalisation (USD)**

\$50M

\$33M

\$250M (E)

\$180M

**Memory
Capacity**

40nm cells achieved
Mb Array by mid-2018

Start work on
Mb Array

8Mb Array

512Kb

Dimension

40nm

40nm

40nm

130nm

**Development
time**

<2 years*

7 years

7 years

>10 years



COMPETITIVE ADVANTAGE



	Weebitnano	4DS	Crossbar	adesto
Materials	Silicon Oxide	Pr, Ca, Mn	Silver	Tellurium
Manufacturability	Production ready materials	Difficult to run in a production Fab	Difficult to run in a production Fab	Difficult to run in a production Fab
Speed	Fast RD & WR	Fast RD no data on WR	Fast RD & WR	Fast RD & WR
Retention	10Y > room temp	No data	10Y @ 85 °C	40Y @ 125 °C
Endurance	10 ⁵ *	10 ³	10 ⁶	10 ⁵
Production cost	Most cost effective process	Higher Cost of manufacturing	Higher Cost of manufacturing	Higher Cost of manufacturing

Based on public information

* moving to 10⁶



Pr, Ce – rare earth Mn Ag, Ca – not fab friendly

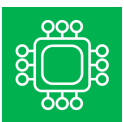
ALLIANCE WITH CEA - LETI

Partnering for highly manufacturable ReRAM



FROM PROTOTYPES TO PRODUCTION

Proven international track record in moving from R&D to production



MEMORY EXPERTISE

Over 10 years of experience in memory technology development



NANOTECHNOLOGY SPECIALIST

State of the art industrial tools



MANUFACTURING ALLIANCES

Over 330 industrial partners



INNOVATION HUB

60+ start-ups in semiconductor, architectures or software



COLLABORATION

Working on 40nm SiO_x development since September 2016



CUSTOMERS

Intel, ST Microelectronics, Globalfoundries



OPENED FRENCH SUBSIDIARY

- Enhances the cooperation with Leti
- Weebit will be eligible for French R&D benefits and tax refunds
- Base for our French employees

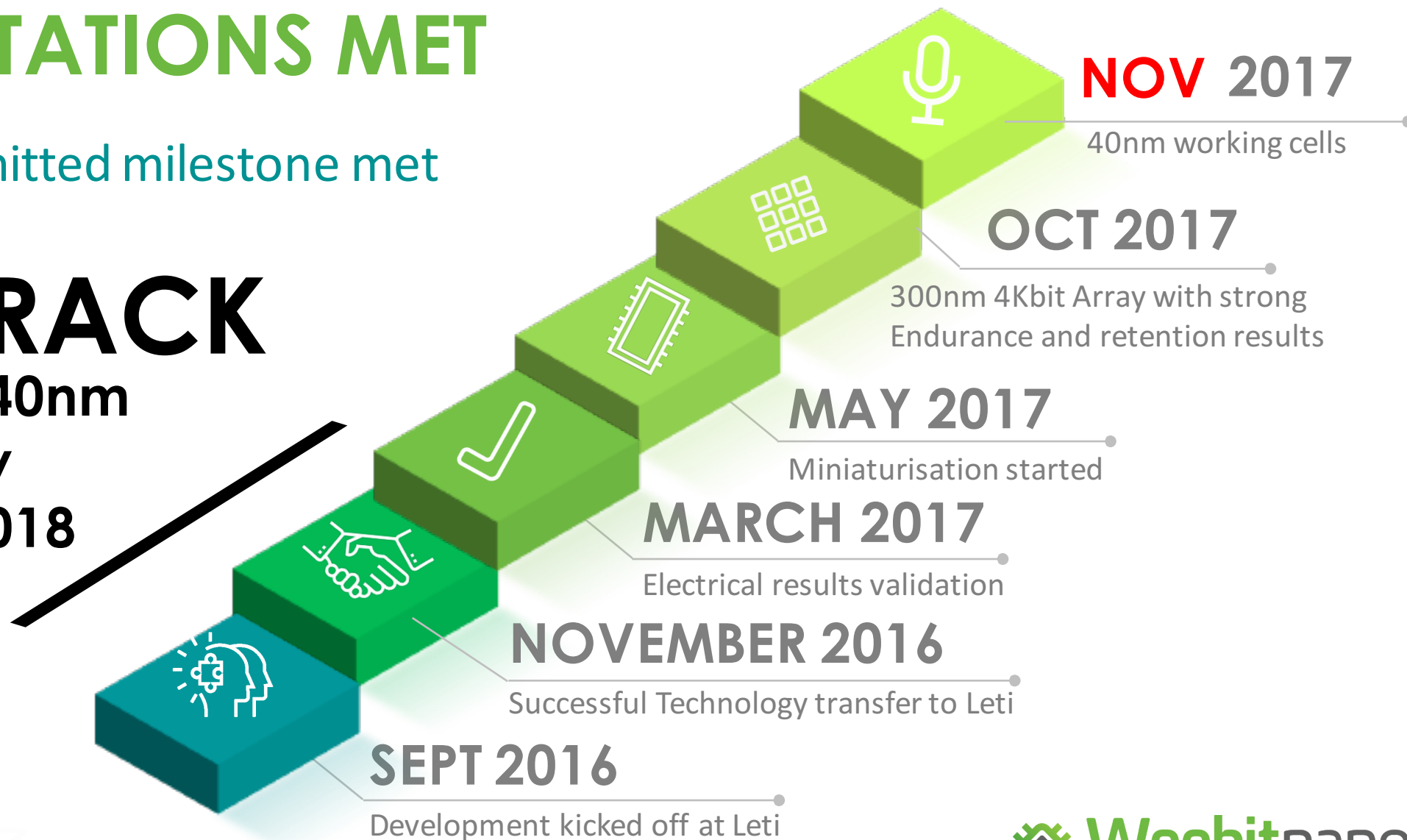


EXPECTATIONS MET

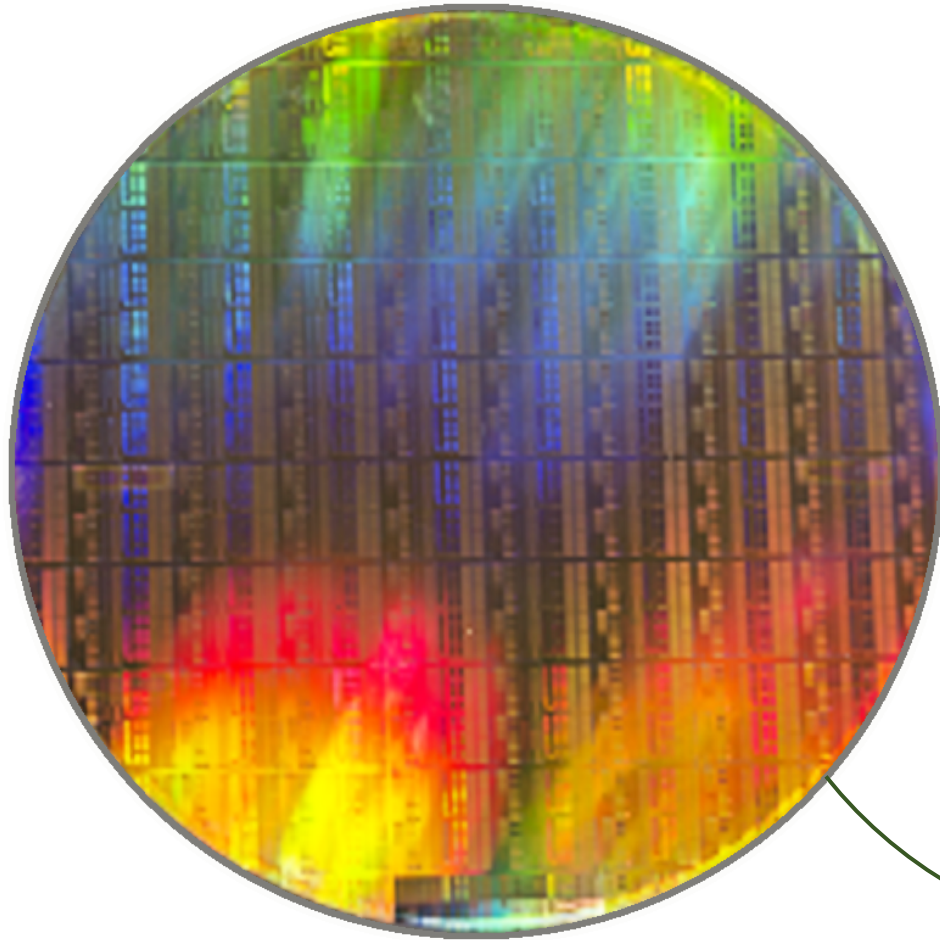
Every committed milestone met

ON TRACK

to reach 40nm
Mbit array
by mid-2018



EXPECTATIONS MET



**40nm
working
cells**

**Demonstrated
one month ahead
of schedule!**

2018 PLANS

TECHNICAL

- Develop a 40nm Mbit array by mid-2018
- Improved Endurance and Retention to meet industry standards by end 2018
- Define a plan and be on the path to develop 2xnm technology

BUSINESS

- Sign first cooperation agreement with a key industry player

DISCLAIMER

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THANK YOU