4DS Memory Limited | ABN 43 145 590 110

Level 2, 50 Kings Park Road, West Perth WA 6005
PO Box 271, West Perth WA 6872

+61 8 6377 8043 | david@4dsmemory.com | www.4dsmemory.com

ASX RELEASE

10 August 2020

Company Update

Key Points

- **Meetings with 4DS, imec and HGST have set the development plan for the next six months**
- **Development plan potentially delivers a megabit chip and/or a corporate transaction in 2021**
- **Following the successful $7.6 million Placement and SPP, the Company is fully funded to implement its strategy**

4DS Memory Limited (ASX:4DS) (**4DS**) (the **Company**), is pleased to summarise a development strategy agreed between the Company, imec and HSGT following a series of discussions over the past few months which culminated in meetings from 27 July to 4 August 2020.

Prior Results

Previous wafer testing results were announced by 4DS on 24 June 2020 and are outlined below:

A. Additional Wafers Lot

Analysis confirmed the highest speed and endurance in the Additional Wafers Lot that have ever been recorded by the Company:

- The best recorded speed at near DRAM speed exceeds Storage Class Memory requirements without the need for speed crippling error correction;
- Endurance is two to three times better than previously reported. Actual endurance may be significantly higher but is currently not quantified due to available lab time and test equipment capacity; and
- The Company also measured retention and the results remain confidential to the Company and its partners until such time as the upper limits of retention can be more accurately defined.

B. Initial Platform Lot

Testing of the Initial Platform Lot validated the integration process steps required to integrate 4DS memory cells with imec's megabit platform. The information gathered from this testing has enabled 4DS to identify which process steps will be further tuned, to benefit future platform iterations.

Future Development

The above results formed the basis of discussions on development strategies which need to be undertaken over the next six months to put the Company in a position to potentially deliver a megabit chip and/or a corporate transaction during 2021.

As such, the Company now proposes to start fabrication of two sets of wafers this quarter on imec production equipment. imec will manufacture one lot of twenty-three (23) Non-Platform Wafers (**Second Non-Platform Lot**) and one lot of twelve (12) Platform Wafers (**Second Platform Lot**).

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The manufacture of these two lots of wafers is a priority for imec.

Second Non-Platform Lot

The Company is defining the process conditions for each of these 23 wafers in collaboration with its partners. These wafers are less complex, faster to fabricate, and easier to test than Platform Wafers, yet can provide valuable input on which process conditions exhibit the biggest improvements in speed, endurance and retention.

Second Platform Lot

Testing process integration in incremental steps is important to define refinements which are needed to reach the Company's goal of manufacturing a fully functional megabit chip with Storage Class Memory characteristics.

The objective of the Initial Platform Lot was to test the integration of dense memory arrays without the complexity of transistors. 4DS validated the integration process, and recent meetings and discussions have identified process steps and conditions that are designed to benefit the fabrication of the Second Platform Lot.

Significantly, the outcome of development discussions is that the Second Platform Lot will be fabricated to contain dense memory arrays with transistors that are able to select memory cells.

This is a major strategic decision to better ensure success in 2021 when, based on the results of this Second Platform Lot, 4DS and its partners will potentially progress to fabricate wafers with all the control logic necessary to read and write selected bits and bytes, and therefore be able to operate as a fully functional megabit memory.

Both lots of wafers will be fabricated with variations of the process conditions from the best wafer in the Additional Wafers Lot, which had exhibited the biggest improvements in speed and endurance in the Company's history.

Timing

The fabrication of both lots of wafers will commence this quarter. Barring any unforeseen equipment problems or new COVID-19 government ordinances, the Second Non-Platform wafers should be available for analysis in mid to late Q4 2020. Due to fabrication complexities related to the inclusion of transistors in the Second Platform Lot, the wafers from the Second Platform Lot are expected to be available for testing in early Q1 2021.

The results from both wafer lots will define the Company's 2021 strategic development plan to achieve its goal of fabrication of a megabit chip and/or a corporate transaction.

COVID-19 Update

The Company continues to monitor COVID-19 restrictions in all the locations in which it operates. If new restrictions are implemented in any location, and to the extent it has a significant effect on Company operations, shareholders will be informed as soon as possible. Currently, there are no restrictions affecting the Company's operations.

Financial and Budget Review

4DS completed a successful Placement and SPP which raised $7.6 million before costs. Those funds, together with $2.5 million in cash as reported in the June 2020 quarterly report, puts the Company in its strongest financial position since listing in late 2015, with sufficient funds to meet its development objectives until end 2021.

Directors, senior management, and service providers received no or reduced salaries from April to June 2020 resulting in a reduction in the quarterly cash outflows. A review of the financial circumstances of the Company and the lifting of restrictions allowing staff to return to the Fremont facilities warrants that salaries return to pre-April 2020 levels, back dated to 1 July 2020.

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As stated above the Company is monitoring COVID-19 in the locations in which it operates and if restrictions are again put in place the Company will review the budget immediately and make the necessary steps to preserve capital.

ENDS

Authorised for release by the Board.

Contact information

Investors: David McAuliffe
4DS Memory
+61 408 994 313
david@4dsmemory.com

About 4DS

4DS Memory Limited (ASX: 4DS), with facilities located in Silicon Valley, is a semiconductor development company of non-volatile memory technology, pioneering Interface Switching ReRAM for next generation gigabyte storage in mobile and cloud. Established in 2007, 4DS owns a patented IP portfolio, comprising 26 USA patents granted and 6 patent applications pending and or filed, which has been developed in-house to create high-density Storage Class Memory. 4DS has a joint development agreement with Western Digital subsidiary HGST, a global storage leader, which accelerates the evolution of 4DS' technology. 4DS also collaborates with imec, a world-leading research and innovation hub in nanoelectronics and digital technologies. The combination of imec's widely acclaimed leadership in microchip technology and profound software and information and communication technology expertise makes them unique.

For more information, please visit www.4dsmemory.com.