

ASX RELEASE

5 October 2022

## COMPANY UPDATE

4DS Memory Limited (ASX:4DS) (**4DS**) (the **Company**) today provides an update regarding the additional internal analysis of the Third Platform Lot.

### Technical Update

On 16 August 2022, the Company reported: “The Company is now performing a Root Cause Action process which includes electrical testing, Transmission Electron Microscopy and material analysis to identify the reason for the difference in results between the Second Platform Lot and the Third Platform Lot”.

The Company has completed its analysis and has identified the modified etch process as the most likely cause of the poor electrical performance of the memory cells used in the imec megabit memory array. 4DS believes that the etch process has induced damage to the crystallinity of 4DS PCMO layer resulting in the write voltage needed to program the cell exceeding the write voltage that the circuitry of the imec megabit memory array could provide. Since prior wafers have shown successful programming of cells of the same size as present in the megabit memory array, the focus will be on further optimizing the etch process to ensure both residue free etching and no crystalline damage to 4DS PCMO layer.

In line with the 2022 agreement with imec, the Company has started discussions with imec to plan the manufacturing of another megabit memory array Platform Lot. Prior to running this Lot, further optimization of the etch process is planned using another short loop. However, it is important to realize, as previously stated, that successful resolution of the etch process can only be demonstrated by electrical tests performed on the Platform Lot after it has been successfully manufactured and delivered to 4DS facilities in Fremont, California. The goal of this next Platform Lot remains the demonstration of the cell operation in a megabit memory array environment and to explore optimized programming conditions to improve both the endurance and retention of 4DS Interface Switching ReRAM cells. Access to the write circuitry of the megabit memory array remains critical to achieve these goals.

Alternatives to the etch process will be explored in parallel, as the probability of a successful optimization of the etch process is unknown. Additional improvements to the memory cell that were demonstrated on wafers processed at the Stanford Nanofabrication Facility will be incorporated in this next Platform Lot, as well.

Detailed timelines of the activities outlined above will be reported to shareholders after the discussions with imec have been completed. This is expected to occur late in October / early November 2022.

***The Company is fully funded to undertake this strategy into 2023.***

### Mr Ting Yen Appointed as Chief Technology Officer

The Board of 4DS is pleased to advise that Mr Ting Yen’s role at 4DS has now changed from Vice President of Engineering to Chief Technology Officer with immediate effect.

Mr Ting Yen has over 30 years of semiconductor experience and is an expert in semiconductor process technology with emphasis on memory architecture / process integration. Ting started his career at the heart of

Silicon Valley with semiconductor pioneers: Fairchild, Hewlett Packard and Philips Research. He then focused his career on memory technology development. He has held key engineering management roles in advanced Research & Development of memory platforms including SRAM, Ternary CAM, Non-Volatile Flash memory and Emerging memory. He has also served as Vice President Engineering for a US based custom foundry wafer fab. Ting holds 21 US Patents and a Master of Science Degree from the University of California, Santa Barbara.

The Board thanks Ting for his commitment to the success of the Company moving forward.

Shareholders can link through to the Investor Hub via: <https://announcements.4dsmemory.com/>

## ENDS

Authorised for release by the Board.

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### About 4DS

4DS Memory Limited (ASX: 4DS), with facilities located in Silicon Valley, is a semiconductor development company of non-volatile memory technology, pioneering Interface Switching ReRAM for next generation gigabyte storage in mobile and cloud. Established in 2007, 4DS owns a patented IP portfolio, comprising 32 USA patents granted (four of which have now expired) and 1 patent application, which have been developed in-house to create high-density Storage Class Memory. 4DS has a joint development agreement with Western Digital subsidiary HGST, a global storage leader, which accelerates the evolution of 4DS technology. 4DS also collaborates with imec, a world-leading research and innovation hub in nanoelectronics and digital technologies. The combination of imec's widely acclaimed leadership in microchip technology and profound software and information and communication technology expertise makes them unique.

For more information, please visit [www.4dsmemory.com](http://www.4dsmemory.com).

### Disclaimer

This release contains certain forward-looking statements that are based on the Company's management's beliefs, assumptions and expectations and on information currently available to management. Such forward looking statements involve known and unknown risks, uncertainties, and other factors which may cause the actual results or performance of 4DS to be materially different from the results or performance expressed or implied by such forward looking statements. Such forward looking statements are based on numerous assumptions regarding the Company's present and future business strategies and the political and economic environment in which 4DS will operate in the future, which are subject to change without notice. Past performance is not necessarily a guide to future performance and no representation or warranty is made as to the likelihood of achievement or reasonableness of any forward-looking statements or other forecast. To the full extent permitted by law, 4DS and its directors, officers, employees, advisers, agents and intermediaries disclaim any obligation or undertaking to release any updates or revisions to information to reflect any change in any of the information contained in this release (including, but not limited to, any assumptions or expectations set out in the release).

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